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Closed loop simulation and hardware implementation of a LED driving circuit from AC source with leakage energy recycling

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Abstract—
This work deals with the design and implementation of an AC to DC LED driving circuit consisting of a buck boost converter and a flyback converter. A buck boost converter is integrated with a fly back converter by sharing a single power switch. A recycling path is also provided to recycle the leakage energy stored in transformer. An EMI filter and a diode bridge rectifier is also included in this converter topology, EMI filter is used to eliminate high frequency current harmonics at the input line. Diode bridge rectifier is used to convert AC source voltage to DC voltage. The control of this single switch is done by using DSPIC 30F2010.This converter has simple structure, low cost, and ease of control as well. In this way, the developed converter can provide high PF and low total harmonic distortion.
The detailed circuit operations and analysis are provided. The theoretical studies and analysis are tested by a prototype of 16-W LED driver with a switching frequency of 60 kHz and also a closed loop simulation is done in MATLAB simulink. The developed converter has maximum power factor of 0.96 and total harmonic distortion of 10.54%
Keywords—Total harmonic distortion (THD), power factor correction (PFC), Leakage energy recycling.

I. Introduction

Because of the green house effect and international petroleum crisis, the whole world put more concentration on efficient energy utilization. But electricity is the one that the users can easily access from wall plugs, batteries, solar cells etc. And nowadays electric applications are used in all where, home appliances, kitchen appliances, lighting appliances etc. The power consumption varies with respect to the application and where it is applied. For the lighting applications, it is 19% of the total electric energy consumed, which is equivalent to approximately 567 billion kWh in the year 2000.

In recent years, the electric energy consumption for lighting applications is much higher than that in 2000 that is near 20% of the total electric energy. Thus, improving the efficiency of lighting applications will save considerable amount of electrical energy. The efficiency of lighting applications depend not only the light sources, materials but also the driving circuits. Comparing with other light sources such as fluorescent lamps, cold cathode fluorescent lamps and high intensity discharge lamps, light emitting diodes (LED) have tremendous advantages [5]. LEDs have ultra long life time (more than 50000 h), low voltage to drive, free from mercury.

And it is very interesting in many automotive, domestic and portable applications. LED lighting systems guarantee high operation security, because they use low voltage levels and no pressured gases are enclosed inside. These systems allow an important cost reduction, because it is not necessary to have any starting circuit. Moreover, the response time is very short (< 100ns) and they can be switched very fast [6]. It is reported that LED is applied for general lighting applications and it is successfully replaced by incandescent lamps and halogen lamps. Consequently, this paper focuses on an innovative driving scheme for LED sources.

Besides batteries, an easy way to acquire electrical energy is from wall plugs. However, for driving LEDs DC supply is required, so a conversion stage from AC to DC is necessary. Among the AC to DC driving circuits for LEDs, switching converter is one of the most popular and economical driving solutions. Conventional ac-to-dc switching converters are composed of a bridge-diode rectifier followed by a bulk capacitor and a dc-to-dc switching converter; this topology has poor performances in power factor (PF) and harmonic distortion. In order to improve both regulations on current harmonics and the PF, an additional PF corrector (PFC) stage is cascaded in front of the traditional converter. In spite of its good performance, such two-stage solutions are usually more expensive and energy inefficient

But for reducing cost and improving efficiency, single stage converters are developed. [13], [14], [16]. These single stage converters have many advantages, but their efficiency is usually not good

enough. Another point to consider is that safety, isolated ac to dc converters are more popular among the LED driving circuits. However, the efficiency is remarkably reduced due to the leakage inductance when applying isolated transformers. [6], [11], [19] To solve this drawback, this paper developing a single stage ac to dc LED driving circuit with a leakage energy recycling mechanism, as shown in Fig. 1.1 Both high pf and high efficiency can be achieved by designing suitable control schemes and circuit parameters

This paper is organized as follows. Section II describes the proposed AC to DC LED driving Converter in which different modes of operations are described. Section III gives the simulation works done in MATLAB Simulink tool. Section IV explains the experimental set up and the results of proposed converter. Section V gives conclusion of the paper.

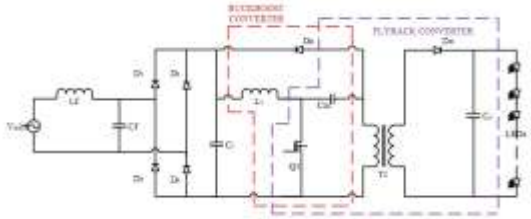

Fig. 1: Proposed AC to DC LED driving circuit configuration

II. Operating principle & circuit analysis

The proposed AC to DC LED driving circuit topology is illustrated in Figure 1. The converter integrates a buck - boost converter with a fly back converter. The buck boost converter work as a PFC cell and also converts the time varying rectified line voltage to a stable dc link voltage which is imposed on a dc link capacitor Cdc. The fly back converter work as a dc dc converter to transfer energy from Cdc to the load which regulate the output voltage and current to the preset values.

The proposed circuit has the characteristics of both a high pf and an excellent output regulation through the series connection between the buck boost PFC cell and fly back cell while sharing a single power switch Q1. Furthermore, the proposed circuit can enhance the efficiency via the innovative structure, which recycles the leakage inductance energy via a freewheeling diode DR and collects in the input capacitor C1.

Since the leakage energy is recycled, the voltage spike can be alleviated. C1 is also helpful in improving electromagnetic interference (EMI), a smaller EMI filter Lf andCf are used to remove high frequency current harmonics from the input line.

Figure 2, shows the theoretical waveforms. To achieve a high pf, the buck boost PFC stage is operated in discontinuous conduction mode (DCM). The fly back stage is also operated in DCM because the power consumption for LED lighting applications is usually less than 200W, the steady state operation can be explained by five modes within one switching cycle.

Details of all operation modes are explained as follows,

2.1 Modes of operation

2.1.1 Mode I:

Fig. 3 shows the equivalent circuit of mode I.

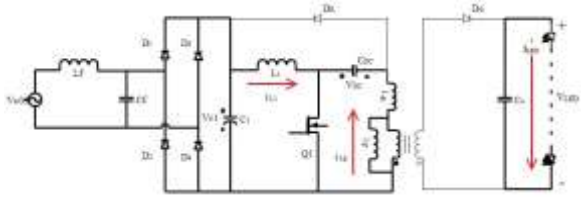

Fig. 3: Mode I equivalent circuit

Mode I begin when the switch Q_1 is switched on, imposing the output of full bridge rectifier (V_{rec}) on the inductor L_1 and d_c link voltage V_{dc} on the primary side inductor L_p. The inductor current i_{L1} and the primary side inductor current i_{Lp} are carried by the switch Q_1. Both the currents i_{L1} and i_{Lp} increases linearly from zero with rising slopes proportional to V_{rec} and V_{dc} respectively, since both L_1 and L_p are operated in DCM to achieve PFC and output regulation. Both i_{L1} and i_{Lp} keep on increasing until Q_1 is switched off, which is the instant both the currents reaches its peak within the switching cycle. On this period secondary current $i_{Ls}(t)$ is zero, that because of the diode in secondary side is reverse biased. So the output capacitor provides the current to the load. When the switch is turned off then moved on to the mode II operation.

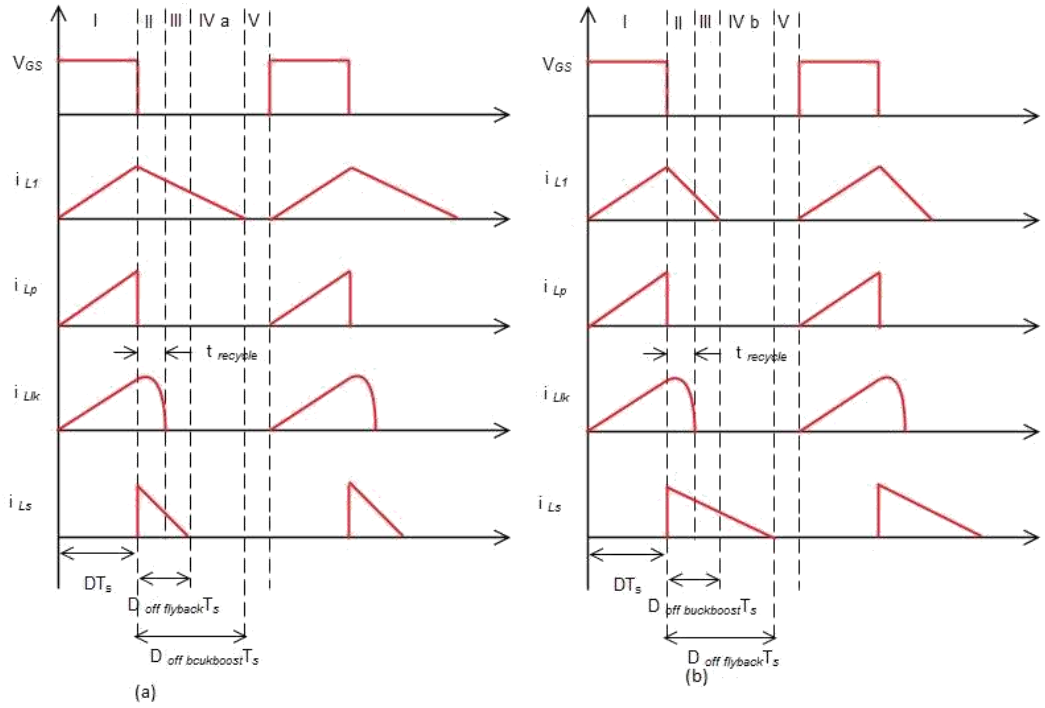

Fig. 2: Theoretical waveforms. (a) At high voltage line. (b)At low voltage line

2.1.2. Mode II:

The transformers are not ideal in real practices, a part of the energy will be stored on the leakage inductor .Fig. 4 shows the equivalent circuit of mode II operation. Here, L_{lk} is the leakage inductance. To prevent transformer saturation and to improve the efficiency, the proposed circuit provides a path to recycle the energy on L_{lk}. In this mode, the L_{lk} current i_{Llk} flows through D_R, and the energy on L_{lk} will be transferred to C_1 simultaneously.

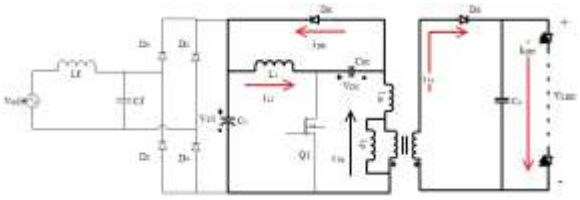

Fig. 4: Mode II equivalent circuit

According to the L-C resonant theory, the leakage energy stored on L_{lk} will be completely transferred to the capac-itance within a quarter of the resonant period. Therefore, the recycling process finishes after

$$t_{recycle} = \frac{1}{4}T_r = \frac{\pi}{2}\sqrt{L_{lk}C_1} \qquad (1)$$

whereT_r is the resonant period,L_{lk} is the total leakage inductance of T_1, and C_1 is the input capacitance. To ensure that the L_{lk} energy is completely recycled, it is important that the off time of Q_1 be larger than $t_{recycle}$. In a typical flyback converter, the voltage spike and ringing exist due to the resonance between L_{lk} and the drain-to-source parasitic capacitance C_{DS} of the power MOSFET. With the proposed energy recycle mechanism, the voltage spike and ringing on Q_1 can be alleviated. D_R is turned on as soon as Q_1 is switched off, and it carries both i_{L1} and i_{Llk}, while i_{L1} and i_{Llk} decline downward to zero separately. Meanwhile, the energy stored on L_1 is discharged to C_{dc} byi_{L1}, and V_{dc} increases accordingly while the L_{lk} energy is recycled to C_1 by i_{Llk}. The energy stored in the transformer core during Mode I will be transferred to the secondary side. During this interval, the output voltage is imposed on the secondary-side inductor L_s, so the secondary-side inductor currenti_{Ls} declines linearly from its peak value which is in proportion to $i_{Lp}$and the transformer turns ratio N. The energy delivered by i_{Ls} not only charges the output capacitor C_o but also supplies current to light up the LED. Mode II ends once i_{Llk} resonates to zero, and the recycling process completes, then mode III begins

2.1.3. Mode III :

Fig. 5 shows the equivalent circuit of the mode III operation. During this mode, i_{L1} and i_{Ls} decline continuously. The down slope of i_{Ls} depends on L_s, i_{Lp} , N, and the output voltage V_{LED}. Moreover, the upslope and peak value of i_{L1} are proportional to V_{rec} at a constant duty ratio. Thus, the duration that iL1 declines to zero varies with V_{rec}. Because V_{dc} is the input voltage of the flyback cell, the upslope and the peak value of i_{Lp} are almost constant. It means that

the down slope and the peak value of the secondary-side inductor current i_{Ls} are also constant if a constant output loading is applied.

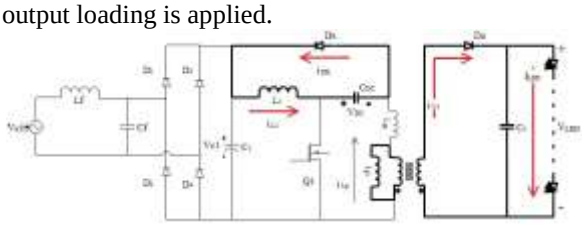

Fig. 5: Mode III equivalent circuit

There are two possible modes following mode III, depending on either the currenti_{L1} or i_{Ls} reaches zero first. If a high line voltage is applied, i_{Ls} reaches zero before i_{L1}. In this case, D_R keeps on conducting and carries i_{L1}; Mode III ends as i_{Ls} decreases to zero, and Mode IV-a begins. On the contrary, i_{L1} decreases to zero earlier than i_{Ls} if the line voltage is low. In this case, Mode IV-b takes over Mode III as i_{L1} decreases to zero.

2.1.4. Mode IV a:

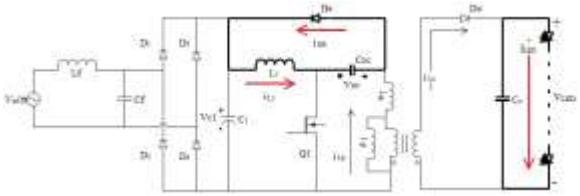

Fig. 6: Mode IV a equivalent circuit

At the beginning of Mode IV-a, i_{Ls} has reached to zero, and C_o supplies the current to light up the LED. At the same time,i_{L1} keeps decreasing until it drops to zero, and the operation proceeds into Mode V.

2.1.5 Mode IV b:

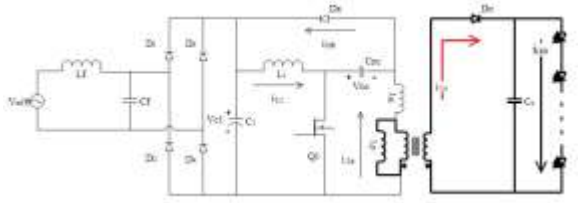

Fig. 7: Mode IV b equivalent circuit

During this mode, i_{Ls} flows through D_o continuously to supply the output LED current. This mode ends when i_{Ls} drops to zero, and the operation enters Mode V.

2.1.6 Mode V:

Throughout this mode, both $i_{L1}$and i_{Ls} are equal to zero while C_o supplies the current to drive the LED. The operation returns to Mode I of the next switching cycle when Q_1 is switched on again. And the cycle repeats again.

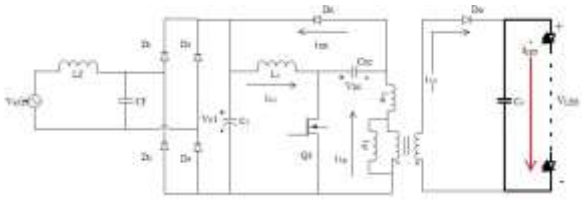

Fig. 8: Mode V equivalent circuit

2.2. Circuit analysis

In order to simplify the theoretical analysis, the following assumptions are made.

(1). Aside from L_{lk}, all other circuit components are ideal.
(2).The capacitance C_1 is small, and V_{rec} is a purely rectified sinusoidal voltage source.
(3).The capacitance C_{dc} is large enough so that V_{dc} considered as a dc voltage source.

From the operating principle explained earlier, both the characteristics of the buck-boost PFC converter and the flyback converter are unaltered, even though they sharing a single common power switch. Therefore, the proposed LED driving circuit can be regarded as two independent conversion stages, that is the buck-boost PFC converter and the flyback converter

2.2.3. Buck - boost pf correction converter :

The LED driving circuit is supplied by the AC line voltage source, its mathematical representation is,

$$v_{ac}(t) = V_m \sin(2\pi f_L t) \qquad (2)$$

where V_m and f_L are the amplitude and frequency of the AC line voltage source respectively. The rectified line voltage is

$$v_{rec}(t) = V_m |\sin(2\pi f_L t)| \qquad (3)$$

Due to the fact that f_L is much lower than the switching frequency f_s, V_{rec} can be regarded as a dc voltage source over a high-frequency switching cycle of the converter.

To ensure the high PF, the buck-boost PFC must be operated in DCM over the entire line-frequency cycle, and therefore, it has to obey the condition as follows:

$$V_{dc} > V_m \frac{D}{1-D} \qquad (4)$$

where V_{dc} and D are the dc-link voltage and the duty

ratio, respectively. Since the buck-boost PFC is operated in DCM, i_{L1} increases from zero once Q_1 conducts and reaches its peak at the end of Mode I. It is noted that the line voltage source supplies a current to the buck-boost PFC converter only during Mode I. The rectified input current i_{rec} is equal to i_{L1} when Q_1 is switched on, and the peaks of i_{L1} are enveloped within a sinusoidal current in phase to the line input voltage when Q_1 is switched on. The peak currents of i_{L1} and i_{rec} can be expressed as

$$i_{L1,peak}(t) = i_{rec,peak}(t) = \frac{V_{rec}(t)}{L_1} DT_s \quad (5)$$

where T_s is the switching period. From (5), the average input current in each switching cycle is,

$$i_{in,avg}(t) = \frac{V_m D^2 T_s}{2L_1} \sin(2\pi f_L t) \quad (6)$$

According to (6), it indicates that the input current is proportional and in phase to the AC line voltage. If the switching frequency and the duty ratio of Q_1 are kept constant over an entire line cycle, a high PF can be achieved.

The input power to the driving circuit can be obtained by taking the average of the instantaneous line power over one line frequency cycle

$$P_{in} = \frac{1}{2\pi} \int_0^{2\pi} v_{ac}(t) i_{in}(t) d(2\pi f_L t) = \frac{V_m^2 D^2 T_s}{4L_1} \quad (7)$$

2.1.3. Flyback converter :

The flyback converter acquires its supply power from the dc-link voltage V_{dc}. Hence, V_{dc} will be imposed on L_p when Q_1 is switched on, and i_{Lp} will reach its peak value i_{Lp}, peak at the end of Mode I, which can be expressed as

$$i_{Lp,peak}(t) = \frac{V_{dc}}{L_p} DT_s \quad (8)$$

To comply with the aforementioned assumption, the flyback converter has to be operated in DCM for satisfying the circuit operation principles, which can be expressed as follows:

$$\frac{N_p}{N_s} \geq \frac{V_m D}{(V_{LED} + V_{Do})(1-D)} \quad (9)$$

where N_p and N_s are the primary and secondary turns of the transformer, respectively, and V_{LED} and V_{DO} are the volt-age drops across the LED load and the diode D_o; respectively. Moreover, since the flyback converter is operated in DCM, the average power of the flyback converter is

$$P_{flyback} = \frac{1}{2} L_p i_{Lp,peak}^2 f_s = \frac{V_{dc}^2 D^2 T_s}{2L_p} \quad (10)$$

Assume that P_{in} is equal to $P_{flyback}$, and V_{dc} can be derived as

$$V_{dc} = V_m \sqrt{\frac{L_p}{2L_1}} \quad (11)$$

Equation (11) demonstrates one key feature of the proposed circuit that V_{dc} is a function of the amplitude of the input voltage. In other words, V_{dc} solely depends on V_m once L_p and L_1 are decided. It is independent of the switching frequency, duty ratio, load condition, etc. Therefore, as long as L_p and L_1 are determined, V_{dc} is fixed and not susceptible to any other parameter variations. On the other hand, after V_{dc} is determined, both the discharging duty ratios of the buck –boost PFC converter and the flyback converter cell, $D_{off;BuckBoost}$ and $D_{off;Flyback}$, respectively, can be calculated as follows:

$$D_{off,Buck\ Boost} = \frac{V_m D}{V_{dc}} \quad (12)$$

$$D_{off,Flyback} = \frac{V_{dc} D}{(V_{LED} + V_{Do})\frac{N_p}{N_s}} \quad (13)$$

Therefore, it can be confirmed whether the buck-boost PFC converter and the flyback converter are operated in DCM. Moreover, since both the buck-boost PFC converter and the flyback converter are operated in DCM, it is crucial to consider the voltage and current stresses on Q_1, D_R, and D_o. According to the operation principles described previously, Q_1 andD_R alternately conduct, leading to the facts that the conducting device carries its maximum current while the nonconducting counterpart bears its maximum voltage stress, and the maxi-mum voltage and current stresses on each device are identical. Therefore, the maximum voltage stresses of Q_1 and D_R, namely, $V_{Q1;max}$ and $V_{DR;max}$, can be estimated as

$$V_{Q1,max} = V_{Dr,max} = V_{m,max}(1 + \sqrt{\frac{L_p}{2L_1}}) \quad (14)$$

Where $V_{m,max}$ and $V_{dc,max}$ are the maximum values of v_m and v_{dc},respectively. On the other hand , both Q_1 and D_R carry the peak current of i_{L1} and i_{Lp}, and the maximum current stresses on Q_1 and D_R , namely $I_{q1,max}$ and $I_{DR,max}$, can be expressed as,

$$I_{Q1,max} = I_{DR,max} = DT_s(\frac{V_m}{L_1} + \frac{V_{dc}}{L_p}) \quad (15)$$

Where $i_{L1,max}$ and $i_{Lp,max}$are the maximum values of i_{L1} and i_{Lp},respectively. The maximum voltage and current stress on D_o, namely,$V_{Do,max}$, can be calculated as

$$V_{Do,max} = V_{dc,max} \frac{N_s}{N_p} + V_{LED} \quad (16)$$

$$I_{Do,max} = i_{Ls,max} = i_{Lp,max} \frac{N_p}{N_s} \quad (17)$$

According to the aforementioned assumptions, the flyback converter acquires energy from a dc voltage source V_{dc}. In accordance with the charge balance theory and the LED model [16]-[18], the relationship between output capacitance C_o and output current ripple can be derived as

$$C_o = \frac{I_{LED}\, DT_s}{\Delta I_{LED}\, R_D} \quad (18)$$

III. Simulation

The performance of the proposed converter was evaluated by computer simulation using MATLAB / Simulink toolbox. The closed loop simulation enabled the converter to provide a constant output voltage.A 48V,16W LED load is con-nected to the output terminals of the converter. The MATLAB model for the proposed converter is shown in fig 9. 16V (V_{rms}) is given as the input supply, The semiconductor switches Q_1 ,shared by both buck boost converter and flyback converter is getting their gate pulses from the relational operator in the feedback subsystem with 30% duty cycle.

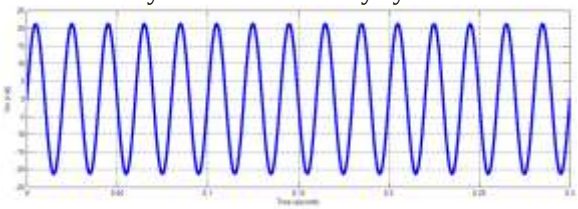

Fig. 10: Waveform of Source voltage

Figure 10 shows the waveform of source voltage , 16V sinusoidal RMS voltage is given as the input to the converter. The corresponding load voltage generated by the converter is shown in figure 11. The converter giving an average load voltage of 48V, which drives the 16 LEDs connected in series

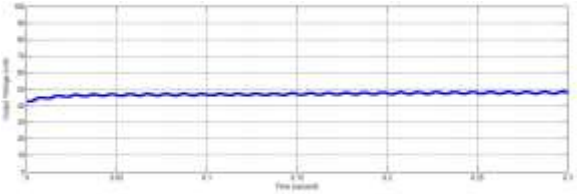

Fig. 11: Waveform of load voltage

Figure 12 shows the current through the inductor in buck boost converter, the buck boost converter is operated in DCM mode to achieve high power factor, that discontinuity of inductor current can be shown in this figure. Figure 13 shows the waveform of current through the primary side of transformer, here the recycling mechanism is coming that clearly shown in that figure. That small spike shown in circle in figure 13 is the recycling part, that is leakage inductance energy.

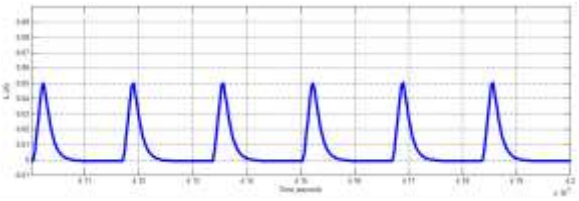

Fig. 12: Waveform of current through the source side inductor

The recycling process initiates once Q1 is switched off. The observed waveform proves that the recycling mechanism functions properly without any deviation from the assumptions and analyses above, and the improvement in efficiency can be achieved.

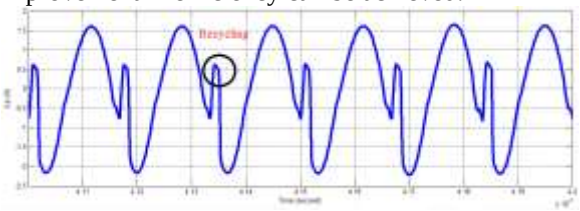

Fig. 13: Waveform of current through the primary of transformer

Figure 14 shows voltage stress across the power semiconductor switch during the given period. The voltage stress is actually very low because of the recycling mechanism, the ripple content is very low.

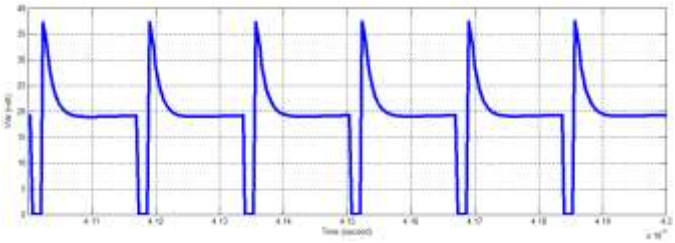

Fig. 14: Waveform of voltage across the power switch Q1

Also, Vdc is a dc voltage with line-frequency ripples. Figure 15 shows the dc link voltage. Although observable spikes of switching noise which can largely be attributed to parasitic effect still exist, the circuit still functions properly.

This recycling process not only enhances the efficiency but also alleviates the spikes and ringing commonly observed in transformer-based converters. Consequently, there is no need to apply any snubber at the cost of efficiency loss.The FFT analysis of the source current to find out the total harmonic distortion in source current. From the FFT analysis, the result obtained that 10.54 %.That shown in figure 16.And the pf obtained as 0.96 for the measurement of pf here using power factor measurement block

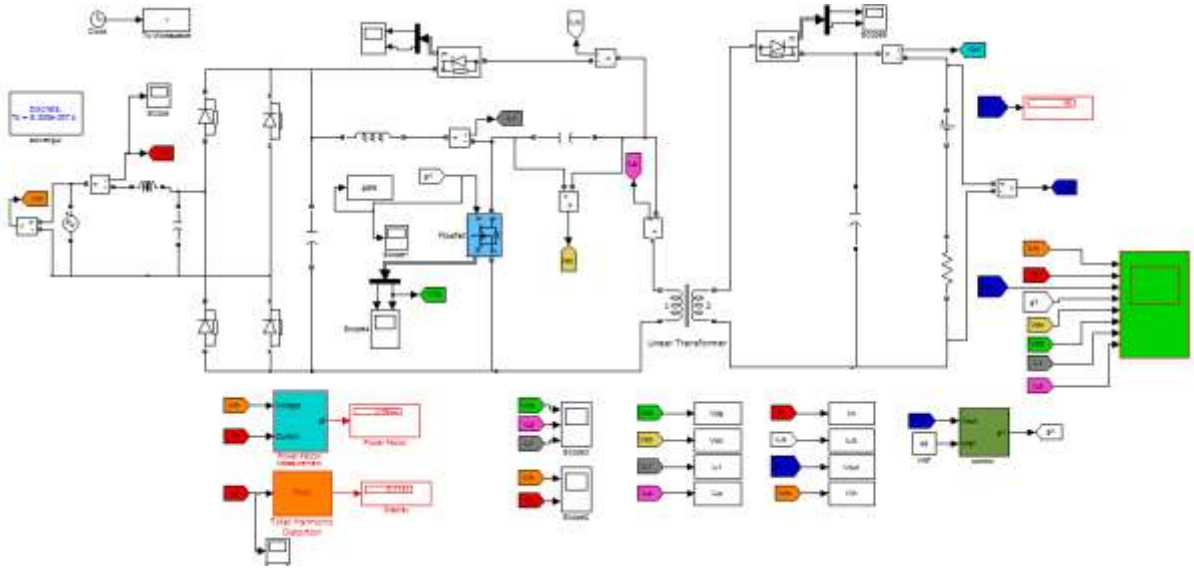

Fig. 9: MATLAB Model

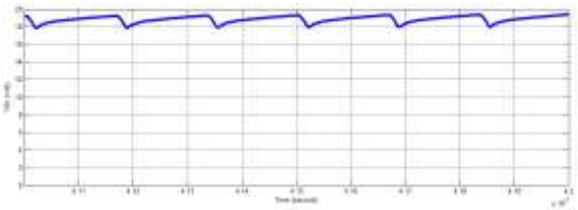

Fig. 15: Waveform of voltage across the dc link capacitor

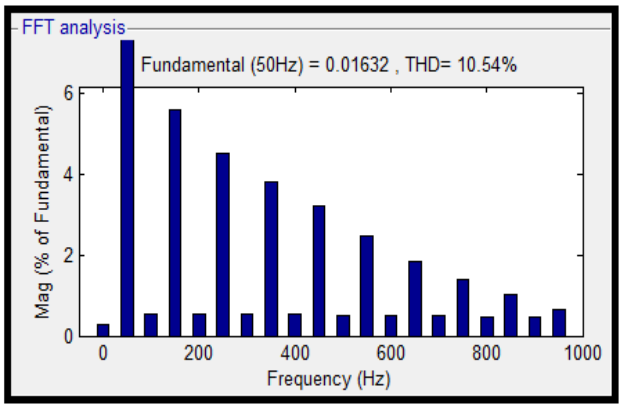

Fig. 16: Total Harmonic Distortion

Component	Specifications
Transformer turns ratio	1
Transformer core	E core
Inductor L_f	2mH
Inductor L_1	150μH
Inductor L_p	150μH
Filter Capacitor C_f	0.1 μF
DC link Capacitor C_{dc}	1 μF
Output capacitor Co	25μF
MOSFET	IRFP250n
Diodes(6 nos.)	BYQ28E
LED load(16 nos.)	1W,3V

TABLE I: Components Used for Power Circuit

IV. Hardware implementation

4.1 Design

To achieve high pf and high efficiency, both the buck boost PFC and fly back converter are operated in DCM. The designed procedures are described as follows, where as the circuit specifications are listed in Table I

Design requirements are

1) Input Voltage : 11-16 V
2) Output Voltage : 48 V
3) Output Power : 16 W
4) Switching Frequency : 60 kHz
5) Maximum duty cycle : 30%

The input side inductor can be calculated as,

$$L_1 = \frac{V_m^2 D^2 T_s}{4P_{in}} = \frac{\left(\sqrt{2} * 15^2\right) * 0.3^2 * 0.85}{4 * 16 * 60 * 10^3} = 0.15mH$$

Before calculating L_p, it is important that the buck boost PFC converter (L_1) be operated in DCM for the high-PF concern. Hence, the ratio of $\frac{L_p}{2L_1}$ has to be decided in advance because it influences V_{dc} and the operation mode. Fig. 4.1, shows the relationship between V_{ac}, $D+D_{off,Buck\ Boost}$, and $\frac{L_p}{2L_1}$. According

to Fig. 17, when $\frac{L_p}{2L_1}$ is larger than 0.5, the buck boost PFC converter (L_1) is operated in DCM. In general, for the component cost and size concerns, V_{dc} is designed as low as possible. Consequently, $\frac{L_p}{2L_1}$ is set to be 0.5, which is large enough to ensure the DCM operation

$$\frac{L_p}{2L_1} = 0.5, \quad L_p = L_1, \quad L_p = L_1 = 0.15mH$$

Aside from L_p, the turns ratio $\frac{N_p}{N_s}$ of the flyback transformer is another dominant parameter to determine whetherthe flyback converter is operated in DCM. From Fig. 18, the flyback converter can be guaranteed to operate in DCM if the entire curve of a certain $\frac{N_p}{N_s}$ is under the CCM/DCM boundary.

In this sample design,$\frac{N_p}{N_s}$ is set to one.

$$\frac{N_p}{N_s} = 1 \qquad N_p = N_s$$

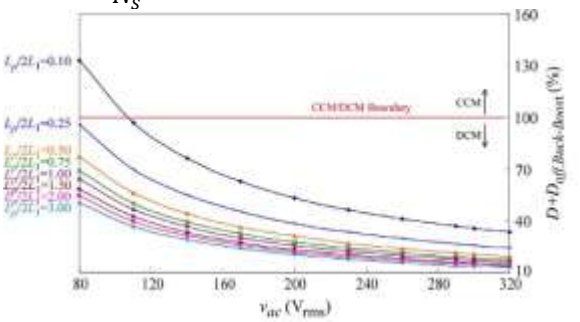

Fig. 17: DCM condition of the buckboost PFC cell

The DC link capacitor can be calculated by using the equation given below,

$$C_{dc} = \frac{P_o * D * T_s}{0.5 * (V_{in}^2 - \Delta V_{in}^2)} = \frac{16 * 0.3 * 2}{60 * 10^3 * (15^2 - 9^2)} \approx 1\mu F$$

Assuming that the desired $4I_{LED}$ is 20% of I_{LED} and R_D is 1 ,Co can be calculated accordingly R_D is 1 , Co can be calculated accordingly

$$C_o = \frac{I_{LED} * D * T_s}{\Delta I_{LED*} R_D} = \frac{0.3333 * 0.3}{0.3333 * 0.2 * 1 * 60 * 10^3} = 25\mu F$$

4.2 Experimental setup

This section describes hardware model and output waveforms of the complete LED driving system.A 48V, 16W LED driving system is developed. Figure 19 shows the complete hardware setup. DsPIC30F2010 is used to generate the control puls. Feedback mechanism also implemented, for that 4N26 opto coupler is used. MOSFET used at here is IRFP250N, for driving this MOSFET TLP250 opto coupler is used. All sections are shown in Fig. 19. 16 LEDs are connected in series to make LED load as shown in Fig 19.

The results obtained from this hardware setup are shown below

Figure.20 shows pwm generated by PIC microcontroller, its duty ratio is 30% and switching frequency is 60kHz. Figure.21 shows the load voltage, it is obtained that average of 48V. Figure 22 shows the load current, figure 23 shows the DC link voltage V_{dc}

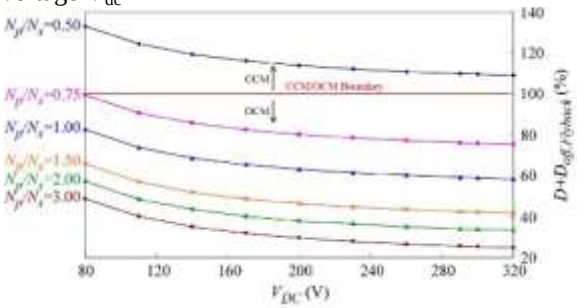

Fig. 18: DCM condition of the flyback converter cell

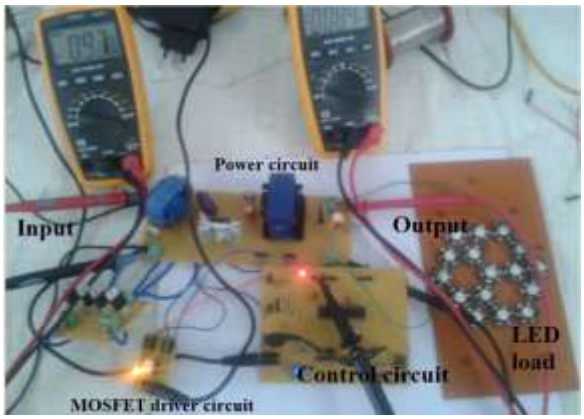

Fig. 19: Experimental prototype of AC to DC LED driving converter

V. Conclusion

A new single-stage high-PF LED driving circuit has been developed. The proposed circuit is based on integrating a buckboost converter for PF correction and a flyback converter for performing output regulation. The new idea of recycling mechanism is implemented. The optimal design of circuit parameters ensures that the circuit can achieve the genuine feature of leakage inductance energy recycling, leading to a
higher efficiency.

The circuit operation is described, and the design equations are derived. A prototype circuit designed for an 16-W LED load is implemented and measured to verify the theoretical analyses, which gives an average output voltage of 48V both theoretical and experimental method. For the controlling of single power semiconductor switch feedback mechanism is used. DSPIC 30F2010 is used

for the PWM generation and the opto coupler TLP 250 is used for MOSFET driving.

Experimental results show that the LED driving circuit meets the design targets, with a PF higher than 0.95 and
a THD less than 16% can be achieved. With this recycling process, the LED driving circuit achieves a maximum efficiency of 90%..The simulation results for 16W MATLAB model,experimental setup and waveforms for the same are studied.

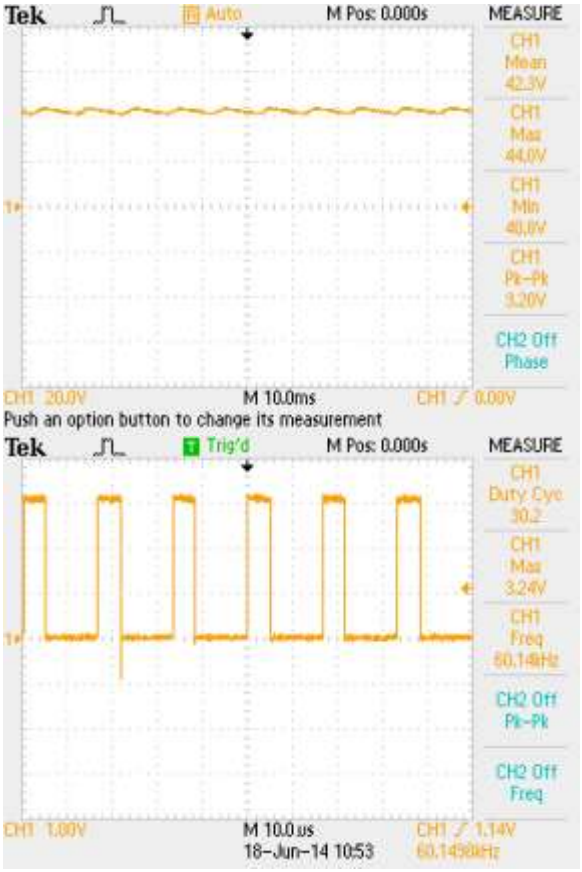

Fig. 20: Pwm signals generated by DsPIC 30f2010

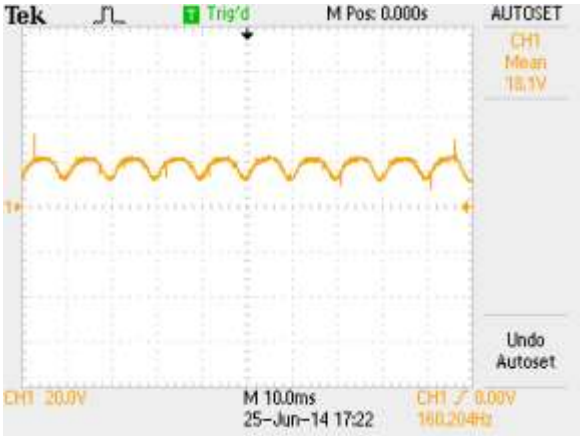

Fig. 23: Waveform of voltage across DC link capacitor

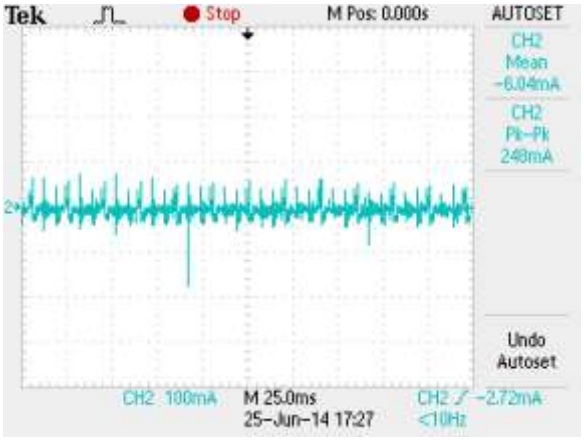

Fig. 22: Load current waveform

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